WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a data input part for receiving a data signal having a prescribed amplitude;

a control part supplying a synchronous signal for capturing said data signal;

a data capturing part for capturing said data signal having said prescribed amplitude and determining said data signal while level-converting said data signal of said prescribed amplitude to an amplitude different from said prescribed amplitude in response to said synchronous signal from said control part; and

a latch part provided independently of said data capturing part for holding said data signal captured in said data capturing part, wherein

said data capturing part is substantially connected to a power source at least when capturing said data signal and determining said data signal.

2. The semiconductor device according to claim 1, including a pair of said data input parts and a pair of said data capturing parts respectively along with single said latch part.

3. The semiconductor device according to claim 1, wherein

said data capturing part has an asymmetrical circuit structure as viewed from said data input part.

4. The semiconductor device according to claim 1, wherein

said data input part includes a data line and an inverted data line,

said data capturing part includes:

a first p-channel transistor having either a source terminal or a drain terminal connected to said power source with remaining said terminal electrically connected to a first node along with a gate terminal connected to said control part, and

a first n-channel transistor having either a source terminal or a drain terminal connected to said first node with remaining said terminal electrically connected to said inverted data line along with a gate terminal electrically connected to said data line,

said latch part includes a first inverter circuit for inverting the potential of said first node, a second node connected to an output terminal of said first inverter circuit and a second inverter circuit connected to said output terminal and an input terminal of said first

inverter circuit,

said first p-channel transistor enters an ON state and said first n-channel transistor enters an OFF state so that said first node reaches a high-level potential and said second node goes low when said data line is low, and

said first p-channel transistor enters an ON state and said first n-channel transistor enters an ON state so that said first node reaches a low-level potential and said second node goes high when said data line is high.

5. The semiconductor device according to claim 4, wherein

the resistance ratio between said first p-channel transistor and said first n-channel transistor is so set that said first node goes low when a current flows to said first p-channel transistor and said first n-channel transistor.

6. The semiconductor device according to claim 4, wherein

said control part includes a transfer gate arranged between said first node of said data capturing part and said first inverter circuit of said latch part and a third inverter circuit for inverting said synchronous signal.

7. The semiconductor device according to claim 4, wherein

said data capturing part further includes a second p-channel transistor arranged between said first p-channel transistor and said first node so that its gate terminal is connected to said data line.

8. The semiconductor device according to claim 4, wherein

said data capturing part further includes:

a third p-channel transistor having either a source terminal or a drain terminal connected to said power source with remaining said terminal connected to said gate terminal of said first n-channel transistor along with a gate terminal connected to said control part, and

a fourth p-channel transistor having either a source terminal or a drain terminal connected to said third p-channel transistor with remaining said terminal grounded along with a gate terminal electrically connected to said data line.

9. The semiconductor device according to claim 8, wherein

said control part includes a third inverter circuit, and

said first p-channel transistor and said third p-channel transistor are driven by said synchronous signal through said third inverter circuit of said control part.

10. The semiconductor device according to claim 4, wherein

said data capturing part further includes:

a third p-channel transistor having either a source terminal or a drain terminal connected to said power source with remaining said terminal connected to said gate terminal of said first n-channel transistor along with a gate terminal connected to said control part, and

a fourth p-channel transistor having either a source terminal or a drain terminal connected to said third p-channel transistor with remaining said terminal electrically connected to said data line along with a gate terminal electrically connected to said data line.

11. The semiconductor device according to claim 10, wherein

said control part includes a third inverter circuit, and

said first p-channel transistor and said third p-channel transistor are driven by said synchronous signal through said third inverter circuit of said control part.

12. The semiconductor device according to claim 1, wherein

said control part includes a first switching element arranged between said data input part and said data capturing part to enter an ON state in response to said synchronous signal when capturing said data signal.

13. The semiconductor device according to claim 12, wherein

said data input part includes a data line and an inverted data line, and

said first switching element includes a second n-channel transistor connected to said data line and a third n-channel transistor connected to said inverted data line.

14. The semiconductor device according to claim 13, wherein

said control part further includes a third inverter circuit for inverting said synchronous signal.

15. The semiconductor device according to claim 1, wherein

said power source includes an internal power source.

16. A display comprising the semiconductor device according to claim 1.

17. The display according to claim 16, including either a liquid crystal display or an organic EL display.